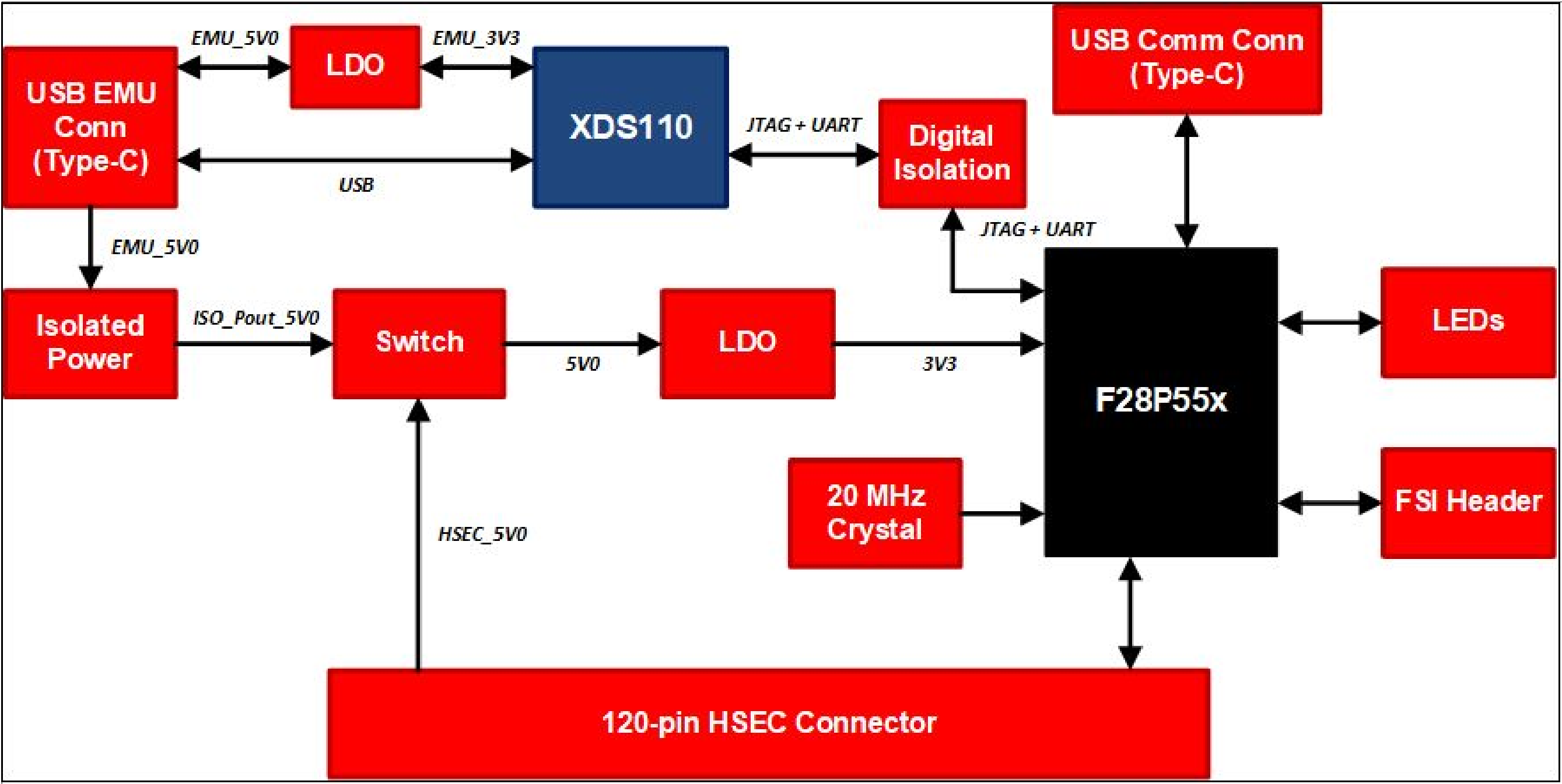


1) USB Differential Pairs - 90 Ohm
(A) XDS_D_P and XDS_D_N
(B) USB_D_P (GPIO41) and USB_D_N (GPIO23)

2) ADC PGA Differential pair Impedance Matching - 50 Ohm
(A) HSEC_PGAx_IN_P pins should match with HSEC_PGAx_IN_N, where x is between 1-3
(B) MCU_PGAx_IN_P pins should match with MCU_PGAx_IN_N, where x is between 1-3

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	Sept 13, 2023	PL	Initial Draft

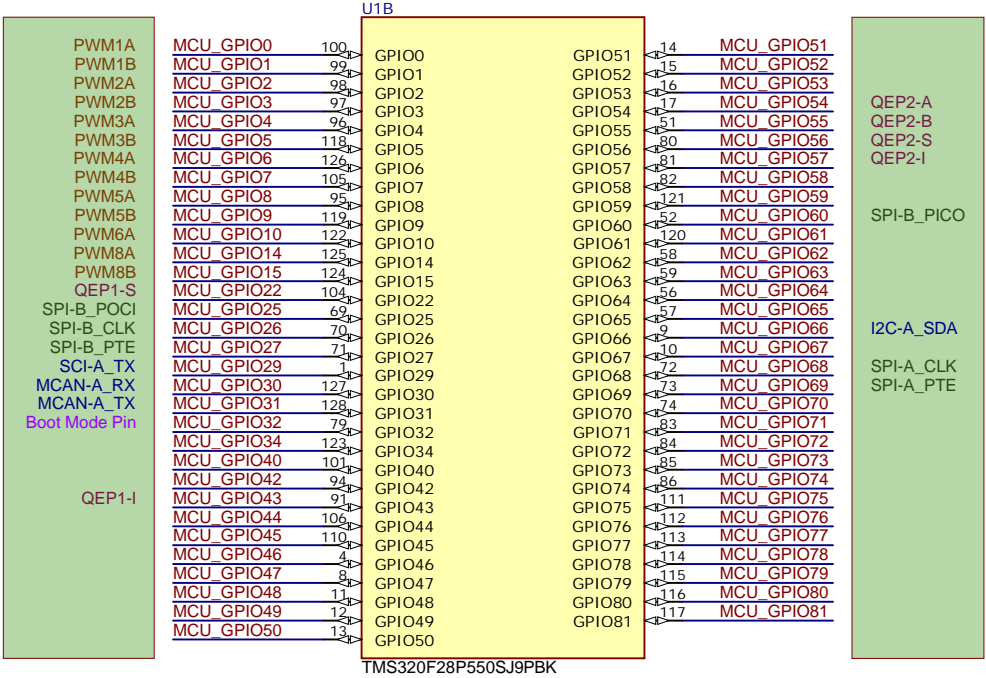
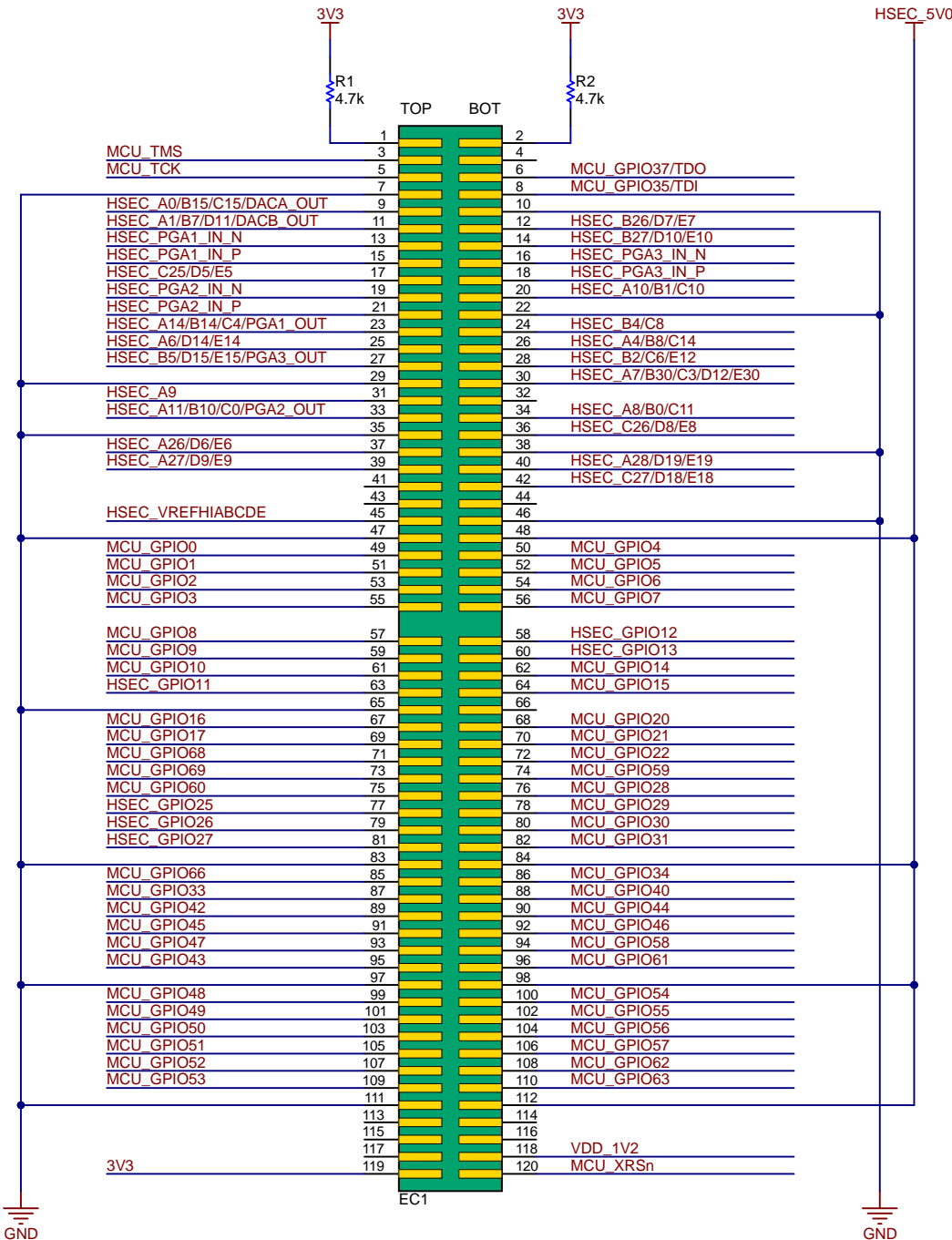
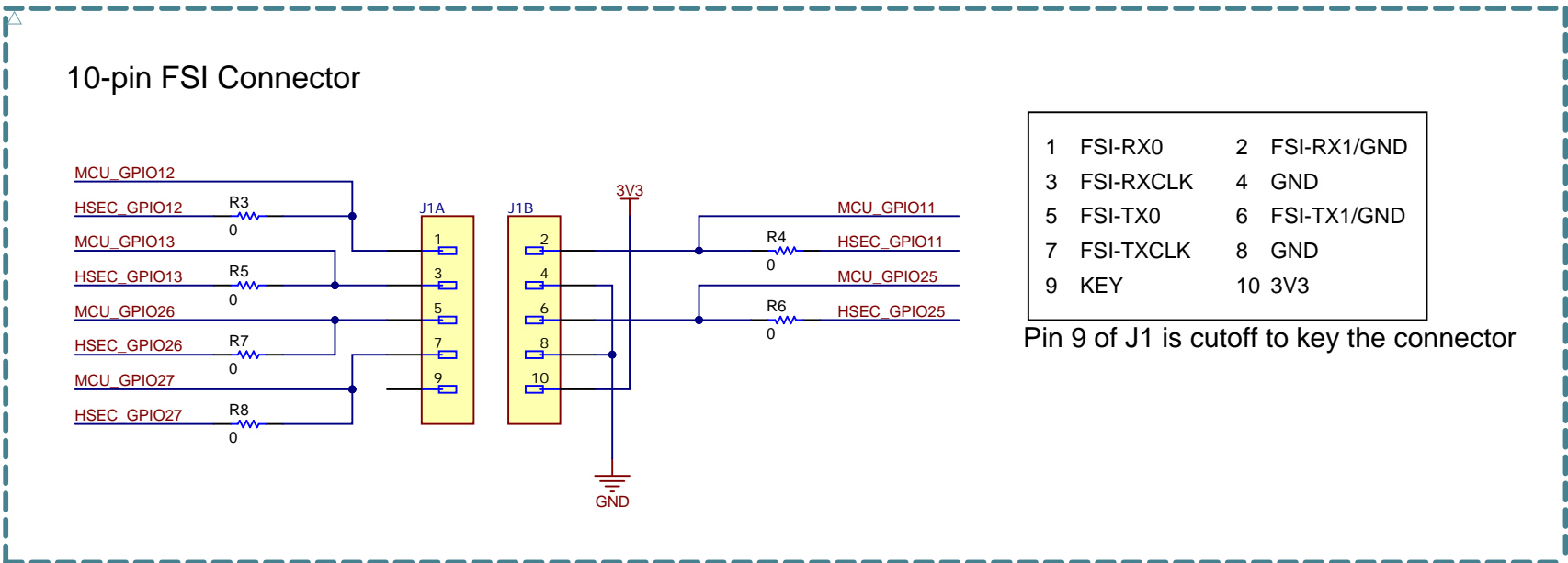


Power to the MCU is either supported by the USB-C on the left or through the HSEC

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Orderable: TMDSCNCD28P55X	Designed for: Public Release	Mod. Date: 10/10/2023
TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: E1	Sheet: 1 of 10
SVN Rev: Version control disabled	Assembly Variant: 001	Size: B
Drawn By: Peter Luong	File: MCU132E1_CoverSheet.SchDoc	
Engineer: Peter Luong	Contact: http://www.ti.com/support	

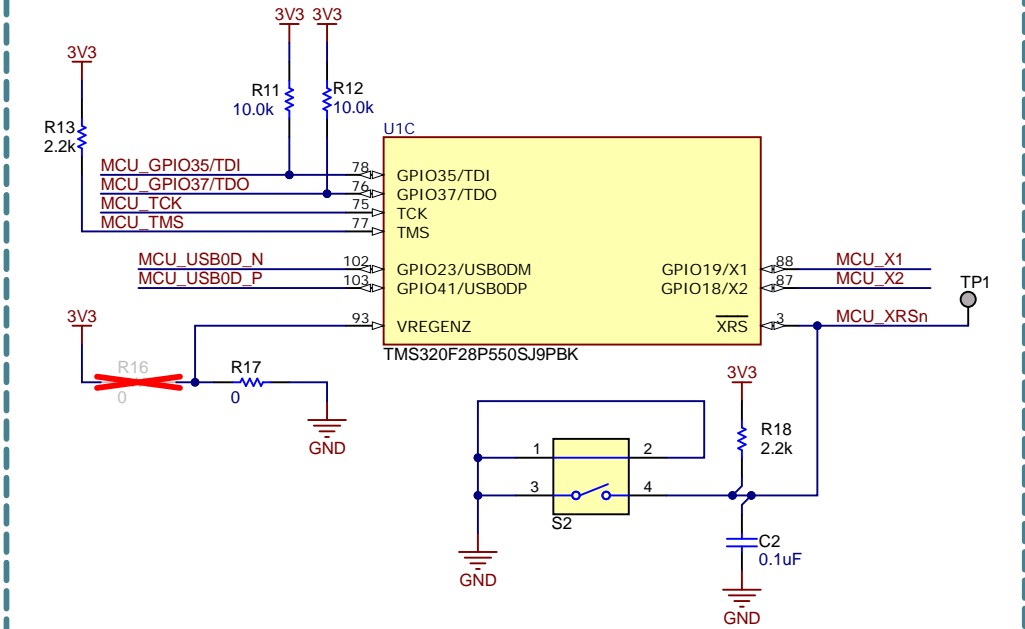
J1 has been updated over previous designs. Pins 9 and 10 were added enabling power to the connector. Additionally Pins 2 and 6, previously GND, have been repurposed to enable the full 3 pin FSI communication. The user can shunt HSEC GPIO11 and HSEC GPIO25 to ground if backwards compatibility is required.



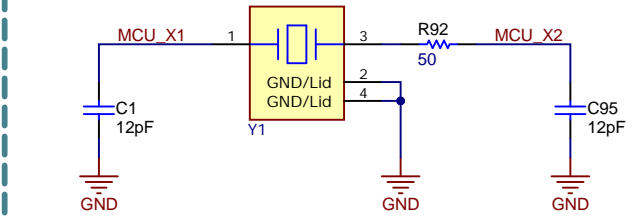
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TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: E1	Sheet: 2 of 10
SVN Rev: Version control disabled	Assembly Variant: 001	Size: B
Drawn By: Peter Luong	File: MCU132E1_GPIO_SchDoc	
Engineer: Peter Luong	Contact: http://www.ti.com/support	

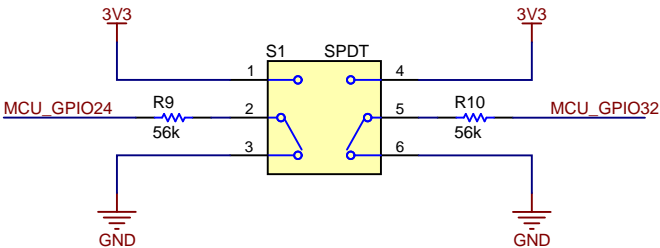
JTAG and Reset



20 MHz External Crystal



Boot Mode Switch

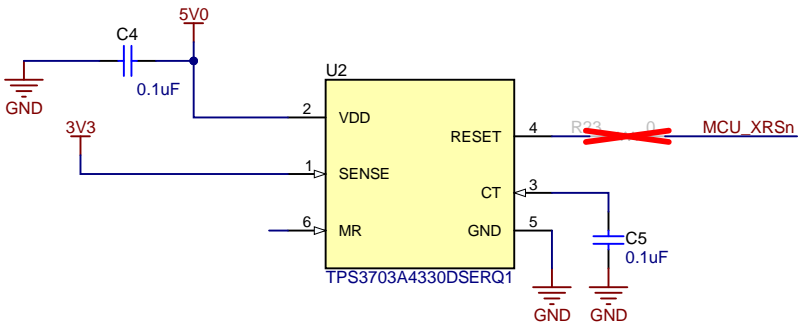


Boot Mode Selection Chart

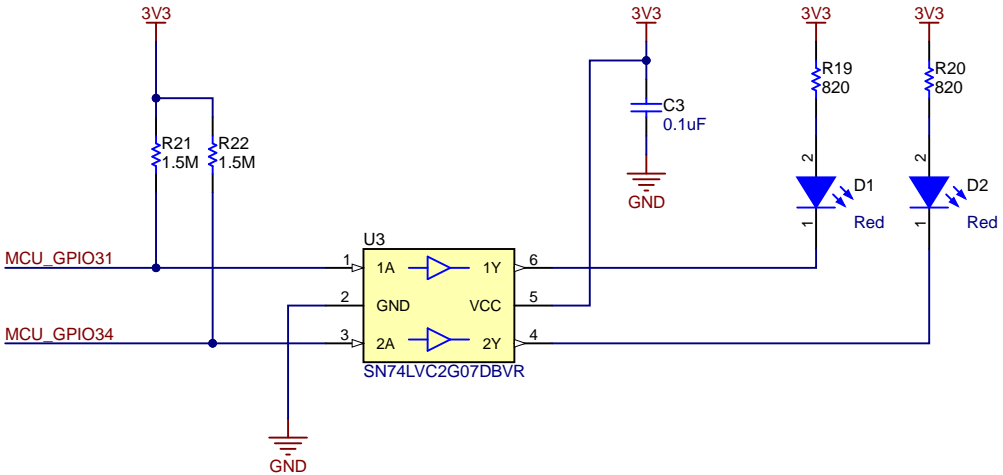
(S2: UP is '1', DOWN is '0')

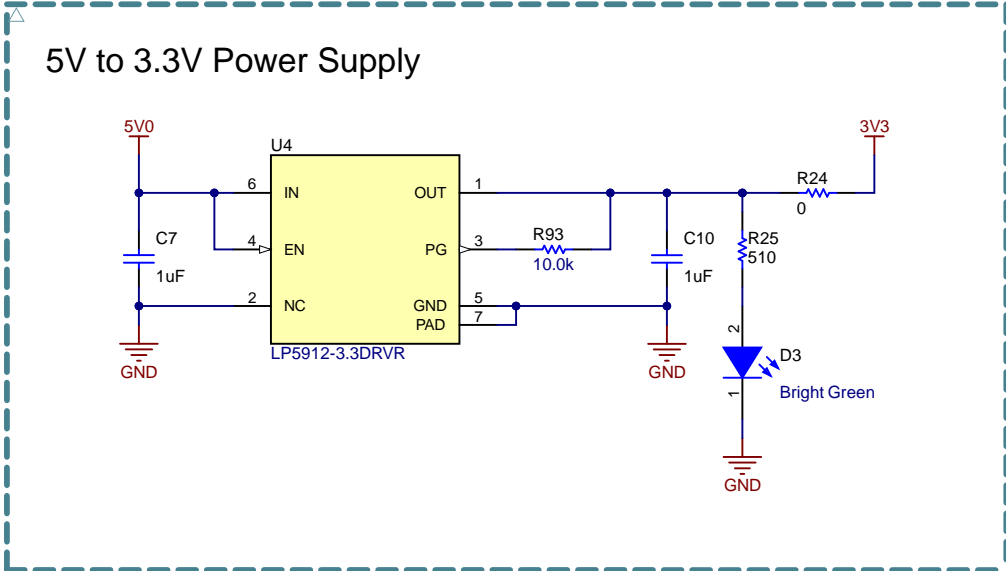
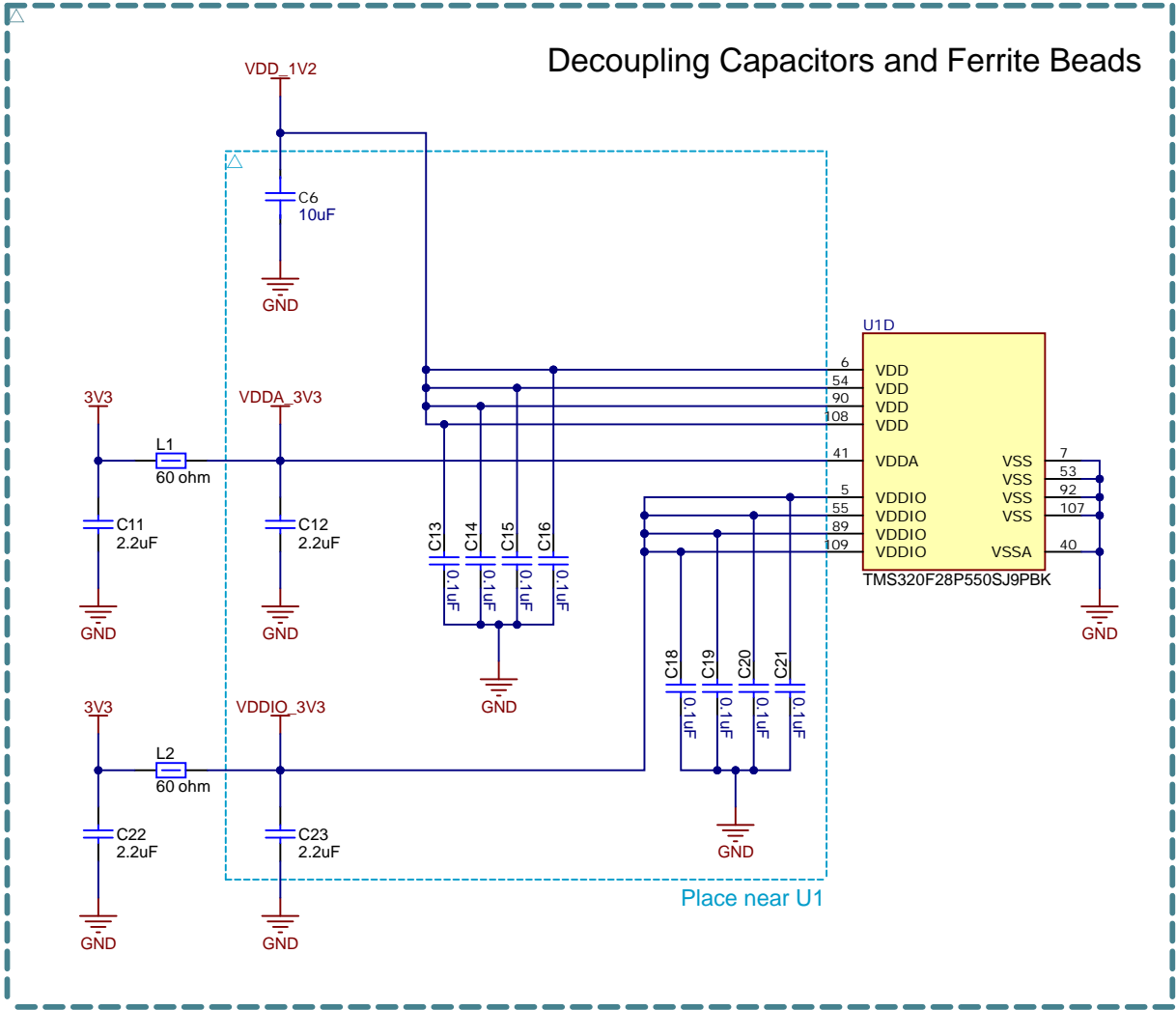
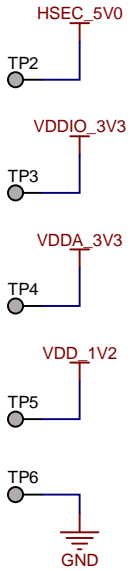
Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN (MCAN-NONFD)
03	1	1	Boot from Flash (USB)

System Supervisory Circuitry



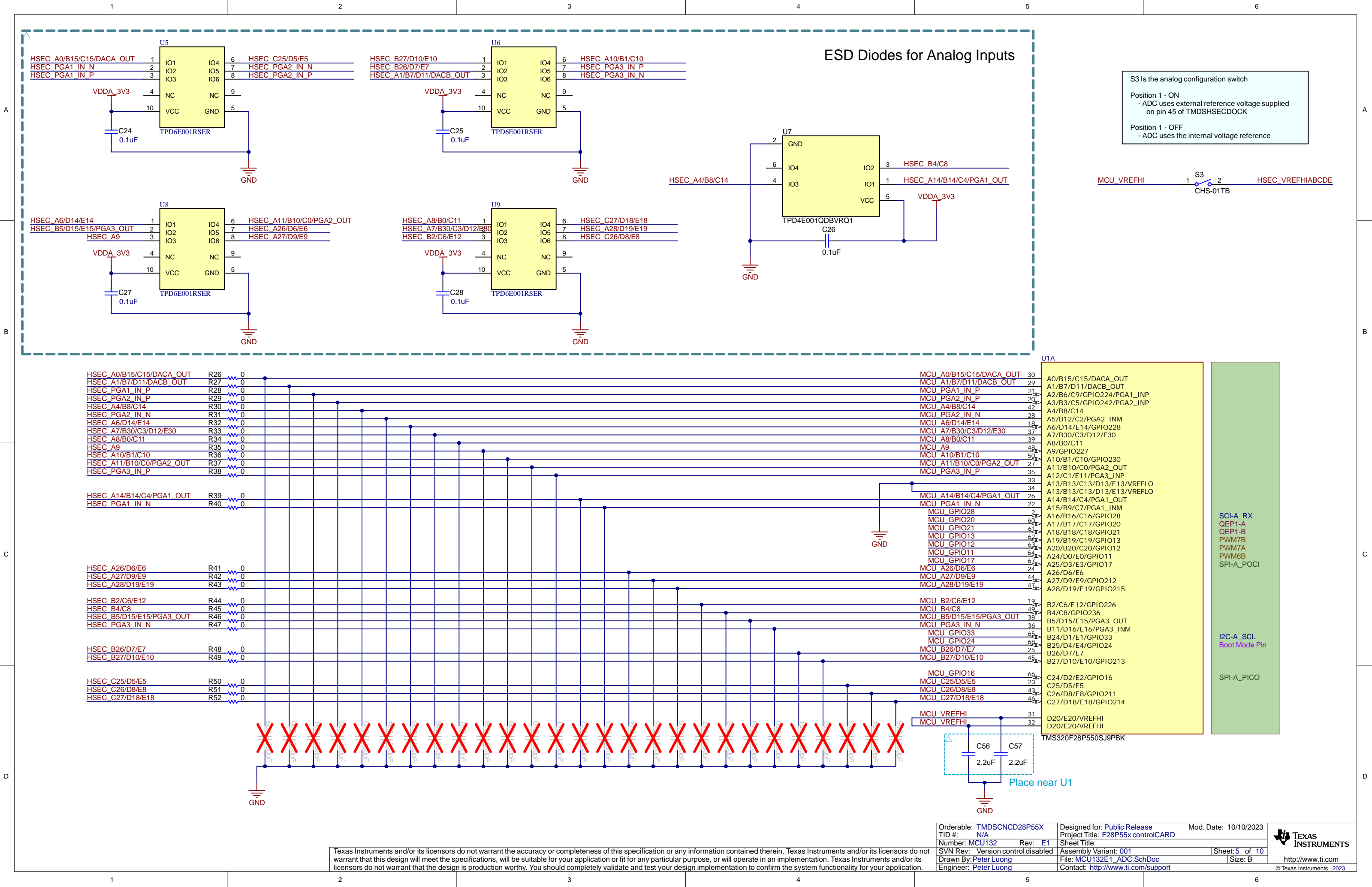
LEDs



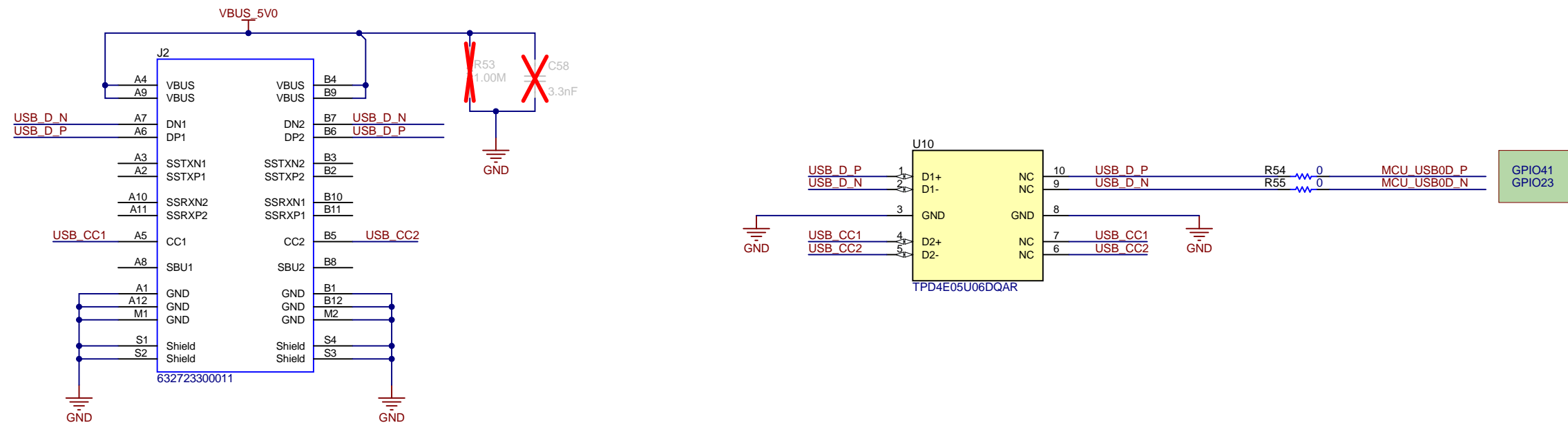


The F28P55x controlCARD uses the internal VREG to generate the 1.2V voltage rail for VDD.

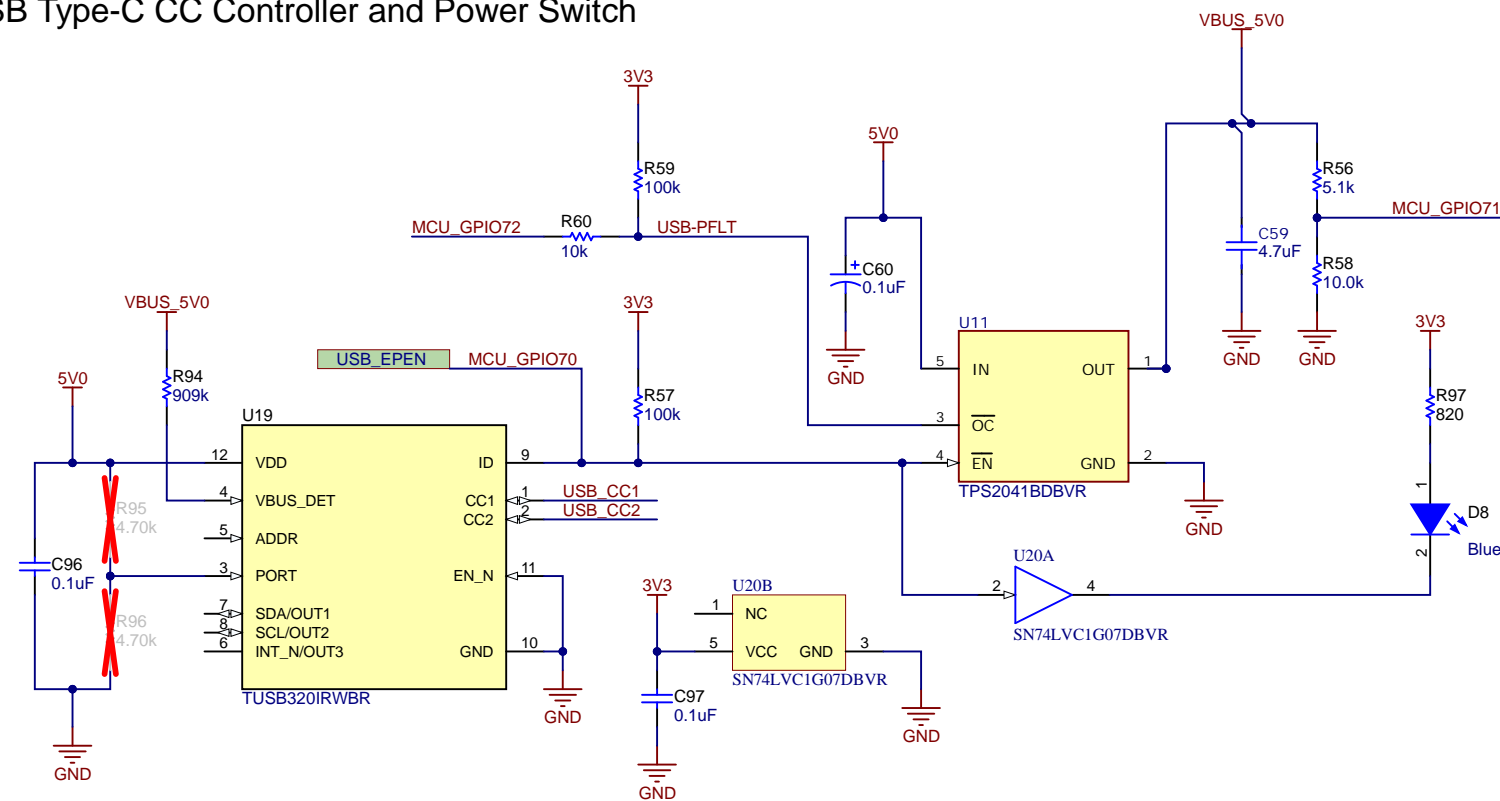
For custom boards using external VREG mode, recommend to use dual-output DC-DC (e.g., TPS62441) to generate both 3.3V and 1.2V supplies.



USB Type-C Connector - Communication Peripheral to MCU



USB Type-C CC Controller and Power Switch



Switch Truth Table		
MCU_GPIO70 STATUS	DESCRIPTION	USB_MODE
1 (HIGH)	UB_CC1 & USB_CC2 are pulled up	Host mode (DFP)
0 (LOW)	UB_CC1 & USB_CC2 are strongly pulled down	Device mode (UFP)

LED D8 will turn on to indicate that the C2000 device is in Host Mode (DFP).

NOTE: USB VBUS_5V0, PFLT & EPEN do not have a specific mux position in this device.

In this controlCARD, a standard GPIO is used to detect changes to these signals.

USB Type-C Connector - XDS110 side

EMU5V0

J3

A4 VBUS B4 VBUS

A9 VBUS B9 VBUS

A7 DN1 B7 XDS_D_N

A6 DP1 B6 XDS_D_P

A3 SSTXN1 B3

A2 SSTXP1 B2

A10 SSRXN2 B10

A11 SSRXP2 B11

A5 CC1 B5 XDS_CC2

A8 SBU1 B8

A1 GND B1

A12 GND B12

M1 GND

GND

S1 Shield

S2 Shield

632723300011

R65 5.1k

EMU_GND

R62 1.00M

C62 3.3nF

EMU_GND

R64 5.1k

EMU_GND

U13

1 D1+ 10 XDS_D_P

2 D1- 9 XDS_D_N

3 GND

4 XDS_CC1

5 XDS_CC2

6 XDS_CC1

7 XDS_CC2

TPD4E05U06DQAR

USB Isolated Power

The diagram illustrates a USB Isolated Power circuit. It features an SN6505BDBVR (U12) configured as a differential line driver. The input side (left) has EMU_5V0 and EMU_GND connections. The output side (right) has EMU_5V0 and EMU_GND connections. The output is coupled to an ISO_Pout_5V0 line through a transformer (T1) and diodes (D9, D10). The output is filtered by capacitors C65 (0.1uF), C66 (10uF), and C67 (0.1uF) to provide a clean 5V output.

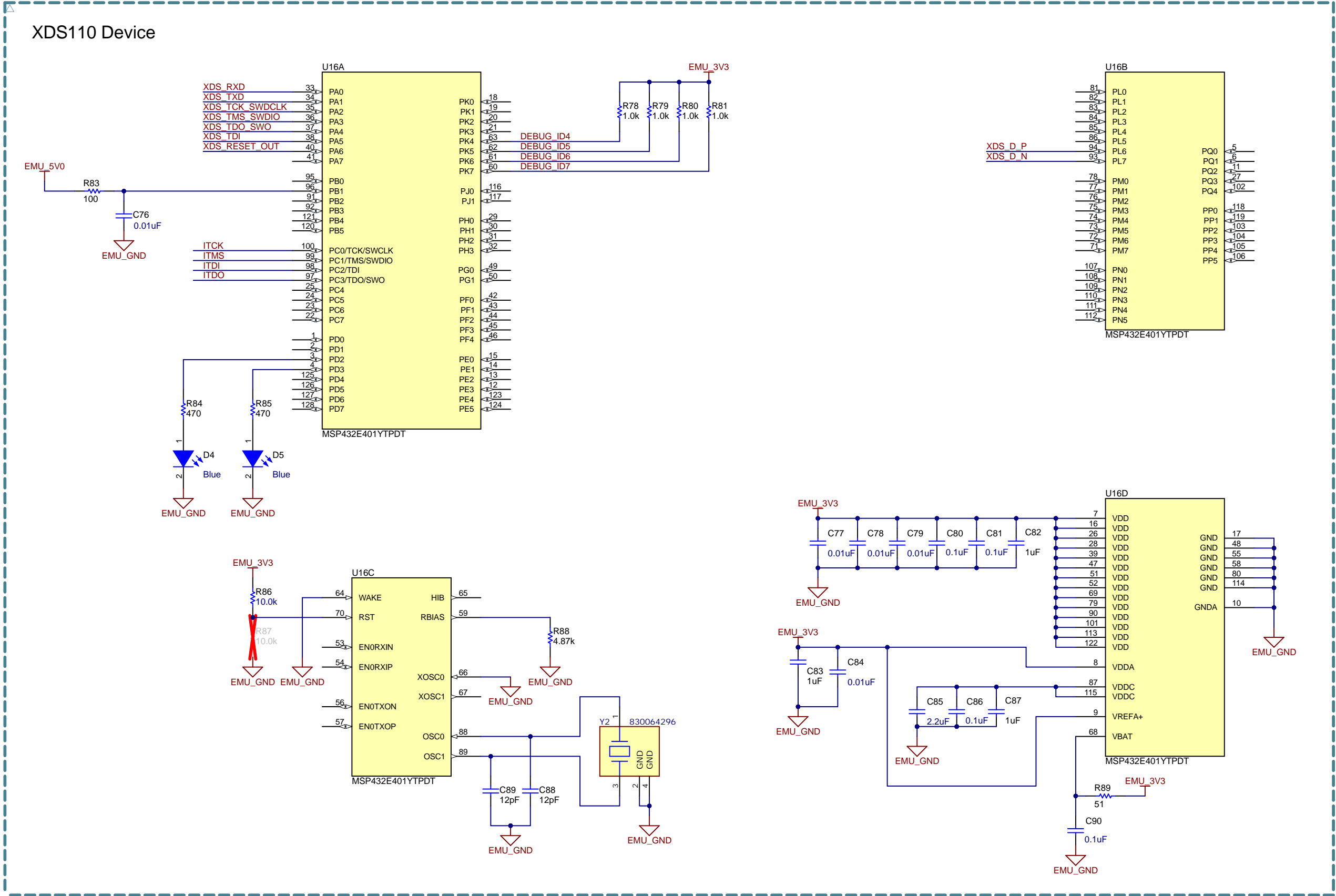
Power Selection Switch

The circuit diagram illustrates a Power Selection Switch using a TPS2113ADRBR IC. The IC is configured with the following components and connections:

- Input Lines:** HSEC_5V0 and ISO_Pout_5V0.
- Capacitors:** C69 (0.1uF) and C70 (10uF) are connected to HSEC_5V0. C71 (0.1uF) and C68 (10uF) are connected to ISO_Pout_5V0.
- Resistors:** R68 (10k) and R69 (10k) are connected to HSEC_5V0. R70 (4.7k) is connected to ISO_Pout_5V0. R73 (1.2k) is connected to VSNS. R72 (430) is connected to ILIM. R71 (1.00k) is connected to the 5V0 supply.
- IC Pins:** IN1 (pin 8), IN2 (pin 6), STAT (pin 1), VSNS (pin 3), ILIM (pin 4), EP (pin 9), and OUT (pin 7).
- Output:** POWER_SWITCH_OUT, which is connected to the OUT pin (pin 7) of the IC.
- LED:** A red LED (D6) is connected to the 5V0 supply and ground.

HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0

HSEC_5V0 > 4V	ISO_Pout_5V0 > HSEC_5V0	POWER_SWITCH_OUT
Yes	X	HSEC_5V0
No	No	HSEC_5V0
No	Yes	ISO_Pout_5V0



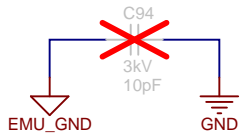
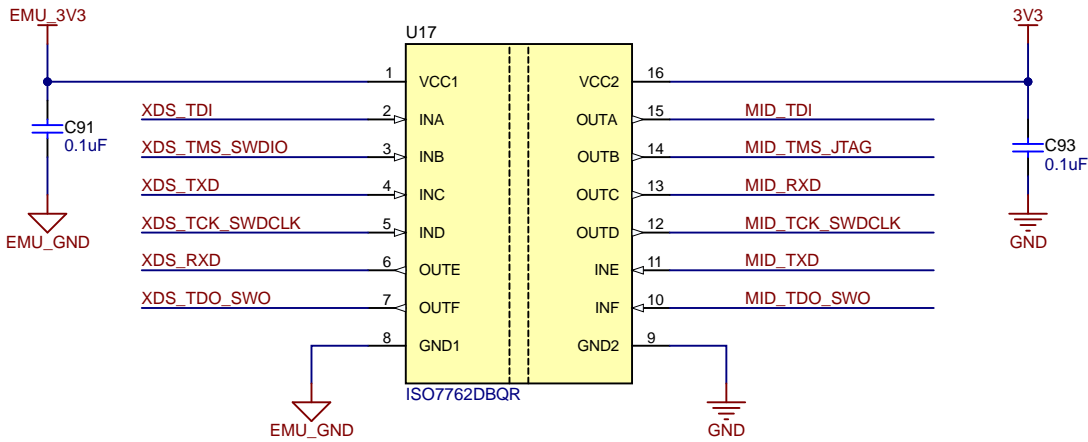
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TID #: N/A	Project Title: F28P55x controlCARD	
Number: MCU132	Rev: E1	Sheet: 8 of 10
SVN Rev: Version control disabled	Assembly Variant: 001	Size: B
Drawn By: Peter Luong	File: MCU132E1_XDS110_MCU.SchDoc	
Engineer: Peter Luong	Contact: http://www.ti.com/support	

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.

(Cold Side)

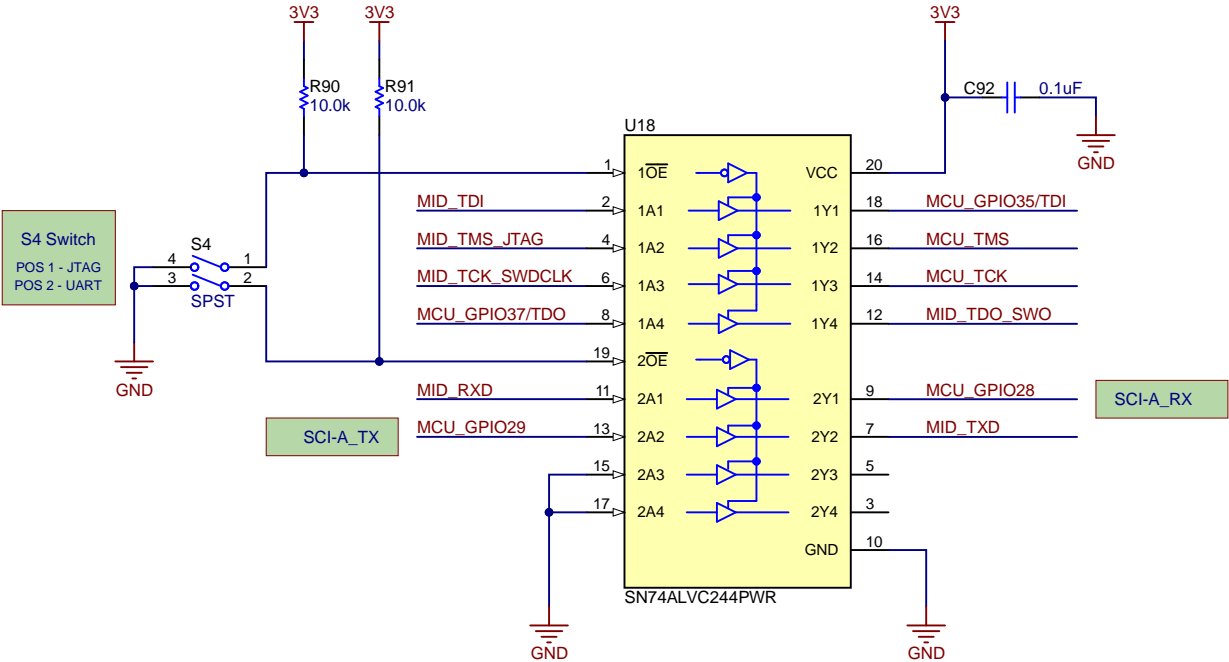
(Hot Side)



WARNING: To avoid potential shock hazard in high-voltage settings, leave the Y cap (C94) unpopulated from the EVM.

S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins





PCB Number: MCU132
PCB Rev: E1

PCB
LOGO
Texas Instruments



PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5
Assembly Note
Clip off KEY pin 9 of J1 connector header

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Number: MCU132	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 10 of 10
Drawn By: Peter Luong		File: MCU132E1_Hardware.SchDoc	Size: B
Engineer: Peter Luong		Contact: http://www.ti.com/support	